Scott Christopher Smith

CONTACT INFORMATION:

University of Arkansas
Department of Electrical Engineering
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ACADEMIC EXPERIENCE:

Ph.D. Computer Engineering, August 1998 – May 2001 (4.0 GPA)
University of Central Florida
Area of emphasis: Computer Architecture and Digital Systems
Advisor: Ronald F. DeMara
Dissertation: Gate and Throughput Optimizations for NULL Convention Self-Timed Digital Circuits
- consisted of developing:
  1) a formal methodology for designing optimal NULL Convention Logic (NCL) asynchronous delay-insensitive digital circuits, which allows for speed/area/power tradeoffs
  2) a formal methodology for designing throughput optimal NCL systems
  3) a technique for reducing the NULL cycle, thus increasing throughput
  4) an NCL 72+32×32 MAC, which outperforms other delay-insensitive/self-timed MACs in the literature

M.S. Electrical Engineering, January 1997 – May 1998 (4.0 GPA)
University of Missouri – Columbia
Area of emphasis: Computers and Digital Systems
Advisor: Michael J. Devaney
Master's Project: Fourier Based Three Phase Power Metering System
- consisted of designing and building a Fast Fourier Transform implementation of a 3-phase power metering system, using a DSP integrated with a 68000 core processor and a communications co-processor

B.S. Electrical Engineering, **B.S. Computer Engineering**, and **Minor in Mathematics**, August 1992 – May 1996
University of Missouri – Columbia
Graduated Magna Cum Laude with a GPA of 3.732
Advisor: Robert McLaren
Senior Project: PLC Controlled Model Railroad

CERTIFICATION:

Passed the EIT (FE) Examination (1996)

AREAS OF EXPERTISE:

Computer Architecture, Embedded Systems, Digital Logic, FPGAs, Asynchronous Logic, NULL Convention Logic, CAD Tools for Digital Design, Computer Arithmetic

WORK EXPERIENCE:

Associate Professor of Electrical Engineering with Tenure (August 2007 – present)
Adjunct Associate Professor of Computer Science & Computer Engineering (September 2008 – present)
University of Arkansas, Department of Electrical Engineering and Department of Computer Science & Computer Engineering
- Taught Digital Design I (ELEG 2903 / CENG 2113) – FS08, FS07
- Taught Digital Design II (ELEG 2913 / CENG 2123) – Sp08, Sp09

Associate Professor of Computer Engineering with Tenure (promoted March 2007, to be effective September 2007)
University of Missouri – Rolla, Department of Electrical & Computer Engineering

Assistant Professor of Computer Engineering (August 2001 – August 2007)
University of Missouri – Rolla, Department of Electrical & Computer Engineering
- Taught Digital Logic (CpE 412) – FS06, FS05, FS04, FS03, FS02
- Taught Digital System Modeling (CpE 318) – WS07, WS06, WS05, WS04, WS03, WS02
- Taught Introduction to Computer Engineering (CpE 111) – FS06, FS05, FS01
- Supervised Computer Engineering Lab I (CpE 112) – WS07, FS06

Graduate Research Assistant (August 1999 – May 2001)
University of Central Florida: NULL Convention Logic (NCL) Project, sponsored by Theseus Logic, Inc.
- Developed formal methodologies for designing optimal NCL circuits and throughput optimal NCL systems

Adjunct Faculty for Computer Engineering (August 1999 – December 1999)
University of Central Florida
- Taught High Performance Computer Architecture (EEL 5708) – FS99
- Instructed over 50 students, including 16 students at 5 off campus locations through taped lectures (FEEDS)

Graduate Research Assistant (May 1999 – August 1999)
University of Central Florida: VMGOES Project, sponsored by U.S. Department of Defense
- Tested neural network vehicle models using MODSAF
- Performed statistical analysis of generated vehicle model data

Graduate Teaching Assistant (August 1998 – May 1999)
University of Central Florida, Department of Electrical & Computer Engineering
- Taught Digital Circuits and Systems Lab (EEL 3342) – WS99, FS98
- Taught Computer Systems Design Lab (EEL 4767) – WS99, FS98

Graduate Teaching Assistant (January 1997 – December 1997)
University of Missouri – Columbia, Department of Electrical & Computer Engineering
- Taught Experimental Electrical Engineering Lab (ECE 255) – FS97, WS97
- Supervised Senior Capstone Design Lab (ECE 398/399) – FS97, WS97

Electrical / Computer Engineering Co-op (July 1996 – December 1996)
Motorola, Inc., Boynton Beach, Florida: Paging Products Group
- Developed and coded InfoFLEX, which is used to broadcast and update information service messages to a large number of subscribed pagers (i.e. information service messages are messages that are received by a large number of pagers, such as sport scores, news, stock prices, etc.)

Electrical Engineering Intern (Summer 1996 and Summer 1995)
St. Louis City Water Division, St. Louis, Missouri
- Worked on PLC design to convert the Chain of Rocks water treatment facility to a SCADA-controlled system
- Assisted with the initial setup of a SCADA system to monitor water filters
- Mapped and created an AutoCad drawing of the Chain of Rocks computer network

Engineering Intern (Summer 1994 and Summer 1993)
Horner & Shifrin, Inc., St. Louis, Missouri
- Created a database for the Horner & Shifrin library
- Surveyed properties and obtained lot information from City Hall
- Downloaded survey data into AutoCad and created AutoCad drawings

PROFESSIONAL SOCIETY MEMBERSHIP:

Institute of Electrical and Electronics Engineers (IEEE)
- Faculty Advisor for the University of Arkansas Student Section of the IEEE (2008 – present)
- Secretary of the St. Louis Section of the IEEE (2007)
- Elected **Senior Member** (2006)
- President of the Rolla Subsection of the St. Louis Section of the IEEE (2004)
- Vice-President of the Rolla Subsection of the St. Louis Section of the IEEE (2003)
- Secretary and Treasurer of the Rolla Subsection of the St. Louis Section of the IEEE (2002)

IEEE Computer Society
IEEE Computational Intelligence Society
- Secretary of the St. Louis Chapter of the IEEE Computational Intelligence Society (2005 – 2007)

American Society for Engineering Education (ASEE)
Sigma Xi: Scientific and Engineering Research Honor Society
Eta Kappa Nu (HKN): Electrical and Computer Engineering Honor Society
Tau Beta Pi: Engineering Honor Society
Golden Key National Honor Society

UNIVERSITY SERVICE:

EE Department Activities (at University of Arkansas)
1) Chair of Communications/DSP Faculty Search Committee (2007 – 2008)
2) Member of General Faculty Search Committee (2007 – 2008 and 2008 – 2009)
3) Member of Undergraduate Recruiting Committee (2007 – present)
4) Member of Graduate Program Committee (2008 – present)
5) Member of Undergraduate Program Committee (2008 – present)

6) Member of ELEG Seminar Series Program Committee (2008 – present)
7) Junior Faculty Mentor for Jingxian Wu (2008 – present)
8) Demonstrated Stair-Climbing Wheelchair for 2 Freshman Engineering Program EE Recruiting Sessions (2008)
9) Demonstrated Stair-Climbing Wheelchair for high school students on University Day (2008)

College of Engineering Activities (at University of Arkansas)
1) Member of Tele Fee Committee (2008 – present)

University of Missouri Activities
1) Reviewer for University of Missouri Research Board Proposals (2003, 2004, 2005, 2007)
2) Reviewer for University of Missouri New Faculty Teaching Scholars Proposals (2006)

Freshman Engineering Activities (at UMR)
1) Freshman Engineering Advisor (2001 – 2003)
2) Preview, Registration, and Orientation (PRO) Program Advisor (2002 – 2007)
   - Advised and registered approximately 200 new Freshman Engineering students
3) Mentored 2 groups of new freshman each year as part of UMR's Opening Week program (2004, 2005, 2006)
4) Participated in making a video on "Classroom Respect" for UMR's Opening Week program (2006)

ECE Department Activities (at UMR)
1) Mentor Graphics Liaison (2002 – 2007)
   - Supervised installation of updated digital design tool suite every 2-3 years (work closely with UMR IT)
   - Supervised Mentor Graphics TA to help solve tool problems
   - Prepared yearly Mentor Graphics license renewal report
2) Library Liaison (2003 – 2007)
3) Integrated Circuit and Logic Design (ICLD) Area Coordinator for the ECE Ph.D. Qualifying Exam (2005 – 2007)
4) CpE Ph.D. Qualifying Exam Revision Committee (2004)
5) CpE ABET Accreditation Committee (2001 – 2002)
6) CpE Undergraduate Studies Committee (2001 – 2007)
7) MTI (Missouri Transportation Institute) Liaison (2005 – 2007)
8) TA Evaluator (2004 – 2007)
   - Evaluated 11 potential ECE TAs as part of UMR's GTA Workshop
9) Recruitment
   - Give numerous departmental tours to prospective ECE students and parents (2002 – 2007)
   - Organized students for and participated in photo shoot for CpE brochure (2004)
   - Represented CpE at the Rolla High School Career Fair (2004)
   - Gave ECE department tour for UMR's President's Day open house (2003)
   - Gave ECE department tour for UMR's Miner Days open house (2003)
   - Presented for CpE at the "Careers in Engineering and Technology" program in Springfield (2002)
   - Supervised ECE department exhibit for Engineers' Week at the St. Louis Science Center (2002)
10) CpE Transfer Student Advisor (2004 – 2007)
11) Faculty Associate for UMR's LEAD program for CpE111 (2005 – 2006)
12) Proctored FE Examination (2002)

PROFESSIONAL SERVICE:

Professional Organization Activities
1) Faculty Advisor for the University of Arkansas Student Section of the IEEE (2008 – present)
2) Secretary of the St. Louis Section of the IEEE (2007)
3) Secretary of the St. Louis Chapter of the IEEE Computational Intelligence Society (2005 – 2007)
4) President of the Rolla Subsection of the St. Louis Section of the IEEE (2004)
5) Vice-President of the Rolla Subsection of the St. Louis Section of the IEEE (2003)
6) Secretary and Treasurer of the Rolla Subsection of the St. Louis Section of the IEEE (2002)

Reviewing Activities
1) Reviewer for *Journal of Electronic Testing: Theory and Applications* (2008)
2) Reviewer for *IEEE Transactions on Education* (2007)
3) Reviewer for *IEEE Transactions on Instrumentation & Measurement* (2007, 2008)
4) Reviewer for *IEEE International Computer Software and Applications Conference* (2007, 2008)
5) Reviewer for *IEEE Transactions on VLSI Systems* (2005, 2006, 2007)
6) Reviewer for *International Conference on Microelectronic Systems Education* (2005, 2007)
7) Reviewer for NSF CCLI Phase 2 proposals (2006)
8) Reviewer for *IEE Proceeding on Computers & Digital Techniques* (2006, 2007)
9) Reviewer for *Journal of Low Power Electronics* (2006)
10) Reviewer for *IEEE Industrial Applications Society Meeting* (2005, 2006)
11) Reviewer for *IEEE Region 5 Technical Conference* (2006, 2007)
12) Judge for *IEEE Region 5 North Area Student Papers Contest* (2006, 2007)

13) Reviewer for *Elsevier's Integration, the VLSI Journal* (2004, 2006)
14) Reviewer for *ASEE Midwest Section Annual Conference* (2005)
15) Reviewer for *2nd International Workshop on Frontiers for Information Technology* (2004)
16) Reviewer for *IEEE Design & Test special issue on Clockless VLSI Design* (2003)
17) Reviewer for *International Joint Conference on Neural Networks* (2003)
18) Reviewer for "*Fundamentals of Digital Logic with VHDL Design*," by Brown and Vranesic (2001)
19) Reviewer for *ASEE Conference* (2000)

Conference Organization Activities

1) Member of Program Committee for *International Conference on Microelectronic Systems Education* (2005, 2007)
2) Session Chair for *IEEE Region 5 Technical Conference* (2007)
3) Session Moderator for *ASEE Midwest Section Annual Conference* (2005)
4) Session Chair for *International Conference on VLSI* (2003, 2004)
5) Session Chair for *International Conference on Embedded Systems and Applications* (2003)
6) Session Chair for *IEEE Computer Society Symposium on VLSI* (2002)

TEACHING:

Graduate-Level Courses

1) Digital Logic at University of Missouri – Rolla (FS06, FS05, FS04, FS03, FS02)
   - Computer Arithmetic Hardware, Design Tradeoffs, Algorithmic State Machines, Asynchronous Logic Design
2) High Performance Computer Architecture at University of Central Florida (FS99)
   - Main, Virtual, and Cache Memory, Pipelining, RISC, CISC, and Networking Architectures

Graduate-Level / Senior-Level Course

1) Digital System Modeling at University of Missouri – Rolla (WS07, WS06, WS05, WS04, WS03, WS02)
   - Digital System Design, Simulation, and Synthesis with VHDL using Mentor Graphics design tool suite

Undergraduate-Level Courses

1) Digital Design II at University of Arkansas (Sp08, Sp09)
   - Mealy and Moore Machine and Algorithmic State Machine Design, Optimization, and VHDL Implementation, Advanced Computer Arithmetic, Introduction to Microcontroller Architecture, Asynchronous Logic Design
2) Digital Design I at University of Arkansas (FS08, FS07)
   - Computer Arithmetic, Boolean Algebra, Combinational Logic Design, Digital Components
3) Introduction to Computer Engineering at University of Missouri – Rolla (FS06, FS05, FS01)
   - Computer Arithmetic, Boolean Algebra, Combinational and Sequential Logic Design, Digital Components
4) Supervised Computer Engineering Lab I at University of Missouri – Rolla (WS07, FS06)
   - Digital Circuit Design using Mentor Graphics Schematic Capture Tool (DA), Hardware Implementation with SSI, MSI, and FPGA Components, Digital Oscilloscope Usage
5) Digital Circuits and Systems Lab at University of Central Florida (WS99, FS98)
   - Digital Circuit Design using Electronics Workbench, Hardware Implementation with SSI and MSI Components
6) Computer Systems Design Lab at University of Central Florida (WS99, FS98)
   - Digital System Design using Motorola 68HC11 Microprocessor, including both Hardware and Software
7) Experimental Electrical Engineering Lab at University of Missouri – Columbia (FS97, WS97)
   - Oscilloscope, DMM, and Signal Generator Usage, Analog Circuit Analysis, Filter Design
8) Supervised Senior Capstone Design Lab at University of Missouri – Columbia (FS97, WS97)
   - Helped students solve both hardware and software problems with their Senior Design Projects

Ph.D. Dissertations Advised

1) Venkat Satagopan, "*Automated Pipelining Optimization, Energy Estimation, and DFT Techniques for Asynchronous NULL Convention Circuits using Industry-Standard CAD Tools*," University of Missouri – Rolla, May 2007.
2) Bonita Bhaskaran, "*Automated Synthesis and NCR Optimization for Asynchronous NULL Convention Circuits using Industry-Standard CAD Tools*," University of Missouri – Rolla, May 2007.

Master's Theses Advised

1) Satish Bandapati, "*Design and Characterization of Asynchronous Delay-Insensitive Arithmetic Components Using NULL Convention Logic*," University of Missouri – Rolla, May 2003.
2) Sareen Devireddy, "*Schematic Capture Design & Power Calculation for NULL Convention Delay-Insensitive Digital Circuits using Mentor Graphics Design Tool Suite*," University of Missouri – Rolla, June 2003.
3) Sasikanth Duggini, "*Design Tools for NULL Convention Logic Circuits*," University of Missouri – Rolla, May 2004.
4) Hiten Dharavat, "*Radiation Testing of COTS CMOS Chips Against Continuous Gamma Radiations*," University of Missouri – Rolla, May 2004 (co-advised with Dr. Akira Tokuhiro in Nuclear Engineering).
5) Anshul Singh, "*Using a VHDL Testbench for Transistor-Level Simulation and Power Calculation of NULL Convention Asynchronous Digital Circuits*," University of Missouri – Rolla, December 2004.

6) Arun Balasubramanian, "*An Asynchronous FPGA for NULL Convention Logic Circuits*," University of Missouri – Rolla, January 2005.
7) Ibrahim Kubilay, "*3D Modeling of String Motion*," University of Missouri – Rolla, May 2006.
8) Ravi Sankar Parameswaran Nair, "*Delay-Insensitive Ternary Logic (DITL)*," University of Missouri – Rolla, August 2007.
9) Samarsen Mallepalli, "*Generic Algorithms and NULL Convention Logic Hardware Implementation for Unsigned and Signed Quad-Rail Multiplication*," University of Missouri – Rolla, August 2007.

Undergraduate Projects Advised

1) Sarah Rosenbaum, Jim Ballmann, Nick Hamilton, and Alexis Sietins, "*Stealth Cam Communications*," Senior Design Project, University of Missouri – Rolla, December 2005.
2) Robert Pangrazio, Eric Peters, and Brad Roberts, "*Human Interface Device - MOKI*," Senior Design Project, University of Missouri – Rolla, December 2005.
3) Jonathan Baldwin, Etenia Ponder, and Lindsay Waters, "*Autonomous Stair-Climbing Wheelchair*," REU Project, University of Missouri – Rolla, Summer 2006.
4) José Martí, Raj Mishra, and Katrina Stevens, "*Developing a Fishing System for Tetraplegics*," REU Project, University of Missouri – Rolla, Summer 2006.
5) Warren Brooks, Steven Ortiz, Adam Kuentzler, and Nicholas Grither, "*Fishing System for Tetraplegics*," Senior Design Project, University of Missouri – Rolla, December 2007.
6) Jessica Rutledge, "*Biomagnetic Imaging with the Selective Minimum Norm Method*," REU Project, University of Arkansas, Summer 2008 (co-advised with Dr. Magda El-Shenawee).
7) Chris Bridges and Faheem Ibrahim, "*Dynamic Power Control and Optimization of Autonomous Stair-Climbing Wheelchair*," Senior Design Project, University of Arkansas, December 2008.

Course Development

1) Digital Design I Lab (ELEG2903L / CENG2113L)
   - Added two new experiments: Combinational Logic Implementation using MUXes and RCA Design (2007)
   - Revised entire lab to emphasize circuit design and utilize Altera DE2 FPGA Boards (2008)
   - Revised course content and lab to include Mealy/Moore machine design and optimization, which was previously taught in Digital II (2009)
2) Digital Design II Lab (ELEG2913L / CENG2123L)
   - Revised entire lab to emphasize complex system design and utilize Altera DE2 FPGA Boards (2008)
3) Digital Design II (ELEG2913 / CENG2123)
   - Integrated material on asynchronous circuit design, as part of an NSF Phase II CCLI grant (2008)
4) Computer Engineering Lab I (CpE112) – at UMR
   - Added three new experiments requiring digital circuit implementation using SSI and MSI components; whereas before all circuits were implemented using an FPGA (2002)
   - Developed a method for implementing digital circuits designed using Mentor Graphics schematic capture tool (DA) on Altera's DE2 FPGA board; and revised all laboratory experiments to be compatible with the new design flow and hardware (2006)
5) Digital System Modeling (CpE318) – at UMR
   - Revised course to emphasize VHDL design for synthesis, which is necessary for circuit implementation as an ASIC or on an FPGA (2002)
   - Integrated material on asynchronous circuit design and optimization, as part of an NSF CCLI grant (2006)
6) Digital Logic (CpE412) – at UMR
   - Significantly expanded course material to include various implementations of computer arithmetic circuits and their design tradeoffs, Algorithmic State Machines (ASMs) for designing complex digital systems, and approximately one month of asynchronous circuit design and optimization topics; whereas before the majority of the material was a review of fundamental digital logic topics (i.e. those from CpE111). These topics were condensed into approximately two weeks of review, so that more interesting graduate-level topics could be studied (2002)
7) Introduction to VLSI (CpE311) – at UMR
   - Integrated material on asynchronous circuit design, as part of an NSF CCLI grant, with assistance from Dr. Waleed Al-Assadi (2006)

SCHOLARLY WORK:

Refereed Journal Publications

1) A. Bailey, A. Al Zahrani, G. Fu, J. Di, and **S. C. Smith**, "Multi-Threshold Asynchronous Circuit Design for Ultra-Low Power," *Journal of Low Power Electronics*, Vol. 4/3, pp. 337-348, December 2008.
2) V. Satagopan, B. Bhaskaran, A. Singh, and **S. C. Smith**, "Energy Calculation and Estimation for Delay-Insensitive Digital Circuits," *Elsevier's Microelectronics Journal*, Vol. 38/10-11, pp. 1095-1107, October/November 2007.

3) V. Satagopan, B. Bhaskaran, W. K. Al-Assadi, **S. C. Smith**, and S. Kakarla, "DFT Techniques and Automation for Asynchronous NULL Conventional Logic Circuits," *IEEE Transactions on VLSI Systems: Special Issue on System on Chip Integration*. Vol. 15/10, pp. 1155-1159, October 2007.
4) **S. C. Smith**, "Design of an FPGA Logic Element for Implementing Asynchronous NULL Convention Logic Circuits," *IEEE Transactions on VLSI Systems*, Vol. 15/6, June 2007.
5) G. K. Venayagamoorthy, **S. C. Smith**, and G. Singhal, "Particle Swarm-Based Optimal Partitioning Algorithm for Combinational CMOS Circuits," *Elsevier's Engineering Applications of Artificial Intelligence*, Vol. 20/2, pp. 177-184, March 2007.
6) S. K. Bandapati and **S. C. Smith**, "Design and Characterization of NULL Convention Arithmetic Logic Units," *Elsevier's Microelectronic Engineering: Special Issue on VLSI Design and Test*, Vol. 84/2, pp. 280-287, February 2007.
7) **S. C. Smith**, "Speedup of NULL Convention Digital Circuits Using NULL Cycle Reduction," *Elsevier's Journal of Systems Architecture*, Vol. 52/7, pp. 411-422, July 2006.
8) **S. C. Smith**, "Development of a Large Word-Width High-Speed Asynchronous Multiply and Accumulate Unit," *Elsevier's Integration, the VLSI Journal*, Vol. 39/1, pp. 12-28, September 2005.
9) **S. C. Smith**, R. F. DeMara, J. S. Yuan, D. Ferguson, and D. Lamb, "Optimization of NULL Convention Self-Timed Circuits," *Elsevier's Integration, the VLSI Journal*, Vol. 37/3, pp. 135-165, August 2004.
10) S. K. Bandapati, **S. C. Smith**, and M. Choi, "Design and Characterization of NULL Convention Self-Timed Multipliers," *IEEE Design and Test of Computers: Special Issue on Clockless VLSI Design*, Vol. 30/6, pp. 26-36, November-December 2003.
11) **S. C. Smith**, R. F. DeMara, J. S. Yuan, M. Hagedorn, and D. Ferguson, "NULL Convention Multiply and Accumulate Unit with Conditional Rounding, Scaling, and Saturation," *Elsevier's Journal of Systems Architecture*, Vol. 47/12, pp. 977-998, June 2002.
12) **S. C. Smith**, R. F. DeMara, J. S. Yuan, M. Hagedorn, and D. Ferguson, "Delay-Insensitive Gate-Level Pipelining," *Elsevier's Integration, the VLSI Journal*, Vol. 30/2, pp. 103-131, October 2001.

Patents

1) Robert Nathan Nelms and **Scott Christopher Smith**, *Selective Call Message Formatting*, U.S. Patent: 6,148,178 November 14, 2000; International Patent: WO9838609 September 3, 1998.
2) Frederick Loring Kampe, **Scott Christopher Smith**, Jheroen Pieter Dorenbosch, and Robert Nathan Nelms, *Reliably Updating an Information Service Message*, U.S. Patent: 6,016,107 January 18, 2000; International Patent: WO9839930 September 11, 1998.
3) Robert Nathan Nelms, Marcus A. Gade, Michael J. DeLuca, Frederick Loring Kampe, and **Scott Christopher Smith**, *Selective Call Device and Method for Battery Saving During Information Services*, U.S. Patent: 5,929,773 July 27, 1999; International Patent: WO9838809 September 3, 1998.
4) **Scott Christopher Smith**, Frederick Loring Kampe, and Jheroen Pieter Dorenbosch, *Insert/Delete Modification of Information Service Message*, International Patent: WO9913658 March 18, 1999.
5) Robert Nathan Nelms, Tom Klein, **Scott Christopher Smith**, and Frederick Loring Kampe, *Performing Updates to Multiple Information Service Topics Using a Single Command*, International Patent: WO9839929 September 11, 1998.

Refereed Technical Conference Publications

1) A. Bailey, J. Di, **S. C. Smith**, and H. A. Mantooth, "Ultra-Low Power Delay-Insensitive Circuit Design," *IEEE Midwest Symposium on Circuits and Systems*, August 2008.
2) B. Hollosi, M. Barlow, G. Fu, C. Lee, J. Di, **S. C. Smith**, H. A. Mantooth, and M. Schupbach, "Delay-Insensitive Asynchronous ALU for Cryogenic Temperature Environments," *IEEE Midwest Symposium on Circuits and Systems*, August 2008.
3) I. P. Dugganapally, W. K. Al-Assadi, V. Pillai, and **S. C. Smith**, "Design and Implementation of FPGA Configuration Logic Block Using Asynchronous Semi-Static NCL Circuits," *IEEE Region 5 Technical Conference*, April 2008.
4) I. P. Dugganapally, W. K. Al-Assadi, T. Tammina, and **S. C. Smith**, "Design and Implementation of FPGA Configuration Logic Block Using Asynchronous Semi-Static NCL," *IEEE Region 5 Technical Conference*, April 2008.
5) M. V. Joshi, S. Gosavi, V. Jagadeesan, A. Basu, S. Jaiswal, W. K. Al-Assadi, and **S. C. Smith**, "NCL Implementation of Dual-Rail 2^s Complement 8×8 Booth2 Multiplier using Static and Semi-Static Primitives," *IEEE Region 5 Technical Conference*, April 2007.
6) S. R. Mallepalli, S. Kakarla, S. Burugapalli, S. Beerla, S. Kotla, P. K. Sunkara, W. K. Al-Assadi, and **S. C Smith**, "Implementation of Static and Semi-Static Versions of a Quad-Rail NCL 24+8×8 Multiply and Accumulate Unit," *IEEE Region 5 Technical Conference*, April 2007.
7) R. S. P. Nair, F. Kacani, R. Bonam, S. M. Gandla, S. K. Chitneni, V. Kadiyala, W. K. Al-Assadi, and **S. C. Smith**, "Implementation of Static and Semi-Static Versions of a Bit-Wise Pipelined Dual-Rail NCL 2^s Complement Multiplier," *IEEE Region 5 Technical Conference*, April 2007.
8) **S. C. Smith** and J. Di, "Detecting Malicious Logic Through Structural Checking," *IEEE Region 5 Technical Conference*, April 2007.

9) J. Di and **S. C. Smith**, "A Hardware Threat Modeling Concept for Trustable Integrated Circuits," *IEEE Region 5 Technical Conference*, April 2007.
10) **S. C. Smith**, "Design of a Logic Element for Implementing an Asynchronous FPGA," *15th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 13-22, February 2007.
11) V. Satagopan, B. Bhaskaran, W. K. Al-Assadi, **S. C. Smith**, and S. Kakarla, "Design for Test Techniques for Asynchronous NULL Conventional Logic (NCL) Circuits," *International Joint Conference on Computer, Information, and Systems Sciences, and Engineering*, December, 2006.
12) V. Satagopan, B. Bhaskaran, W. K. Al-Assadi, and **S. C. Smith**, "Automation in Design for Test for Asynchronous Null Conventional Logic (NCL) Circuits," *12th NASA Symposium on VLSI Design*, paper 3.1, October, 2005.
13) B. Bhaskaran, V. Satagopan, and **S. C. Smith**, "High-Speed Energy Estimation for Delay-Insensitive Circuits," *International Conference on Computer Design*, pp. 35-41, June 2005.
14) A. Singh and **S. C. Smith**, "Using a VHDL Testbench for Transistor-Level Simulation and Energy Calculation," *International Conference on Computer Design*, pp. 115-121, June 2005.
15) B. Bhaskaran, V. Satagopan, W. Al-Assadi, and **S. C. Smith**, "Implementation of Design For Test for Asynchronous NCL Designs," *International Conference on Computer Design*, pp. 78-84, June 2005.
16) G. Singhal, G. K. Venayagamoorthy, and **S. C. Smith**, "An Optimal Partitioning Algorithm for Combinational CMOS Circuits Using Particle Swarm Optimization," *14th IEEE North Atlantic Test Workshop*, pp. 87-92, May 2005.
17) **S. C. Smith**, "Designing NULL Convention Combinational Circuits to Fully Utilize Gate-Level Pipelining for Maximum Throughput," *International Conference on VLSI*, pp. 407-412, June 2004.
18) **S. C. Smith**, "Design of a NULL Convention Self-Timed Divider," *International Conference on VLSI*, pp. 447-453, June 2004.
19) **S. C. Smith**, "Completion-Completeness for NULL Convention Digital Circuits Utilizing the Bit-wise Completion Strategy," *International Conference on VLSI*, pp. 143-149, June 2003.
20) S. K. Bandapati and **S. C. Smith**, "Design and Characterization of NULL Convention Arithmetic Logic Units," *International Conference on VLSI*, pp. 178-184, June 2003.
21) **S. C. Smith**, "Speedup of Self-Timed Digital Systems Using Early Completion," *IEEE Computer Society Annual Symposium on VLSI*, pp. 107-113, April 2002.
22) **S. C. Smith**, R. F. DeMara, J. S. Yuan, M. Hagedorn, and D. Ferguson, "Speedup of Delay-Insensitive Digital Systems Using NULL Cycle Reduction," *10th International Workshop on Logic and Synthesis*, pp. 185-189, June 2001.
23) **S. C. Smith** and M. J. Devaney, "Fourier Based Three Phase Power Metering System," *17th IEEE Instrumentation and Measurement Technology Conference*, Vol. 1, pp. 30-35, May 2000.

Refereed Educational Conference Publications

1) **S. C. Smith**, W. K. Al-Assadi, and J. Di, "Integrating Asynchronous Digital Design into the Undergraduate Computer Engineering Curriculum Throughout the Nation," *NSF CCLI PI Conference*, August 2008.
2) **S. C. Smith** and W. K. Al-Assadi, "Integrating Asynchronous Digital Design and Testing into the Undergraduate Computer Engineering Curriculum," *6th ASEE Global Colloquium on Engineering Education*, October 2007.
3) **S. C. Smith** and W. K. Al-Assadi, "Integrating Asynchronous Digital Design and Testing into the Undergraduate Computer Engineering Curriculum," *ASEE Annual Conference & Exposition*, June 2007.
4) **S. C. Smith** and W. K. Al-Assadi, "Teaching Asynchronous Digital Design in the Undergraduate Computer Engineering Curriculum," *IEEE Region 5 Technical Conference*, April 2007.
5) **S. C. Smith**, "Integrating Asynchronous Digital Design into the Undergraduate Computer Engineering Curriculum," *ASEE Midwest Section Annual Conference*, September 2006.
6) **S. C. Smith**, "Group Selection in a Senior/Graduate Level Digital Circuit Design Course," *ASEE Midwest Section Annual Conference*, September 2005.

Industry Seminar

- **S. C. Smith**, "Asynchronous Circuits to the Rescue," Altera Corporation, San Jose, CA, June 14, 2006.

Conference Workshops

- **S. C. Smith**, W. K. Al-Assadi, and J. Di, "Introduction to Asynchronous Circuits and NULL Convention Logic (NCL)," World Congress in Computer Science, Computer Engineering, and Applied Computing, July 2008.
- **S. C. Smith**, W. K. Al-Assadi, and J. Di, "Introduction to Asynchronous Circuits and NULL Convention Logic," *IEEE Region 5 Technical Conference*, April 2007.

GRANTS: Total: $1,426,162; Total as PI: $633,305; Total Share: $587,423 (41%)

1) J. Di (50%), **S. C. Smith (40%)**, and J. P. Parkerson (10%), "SEU/SEL Resistant Ultra-Low Power Asynchronous Processor Design for Low-Temperature Applications," NASA SBIR Phase I through Space Photonics, Inc., $33,317, February 2009 – July 2009.
2) J. Di (50%), **S. C. Smith (35%)**, and H. A. Mantooth (15%), "DIMLOG: Ultra-Low Power Delay-Insensitive Asynchronous Circuits," DARPA, $305,326, October 2008 – March 2010.

3) **S. C. Smith (25%)** and B. Driskill (75%), "Automated Bit-Wise Completion for Asynchronous NULL Convention Digital Circuits," University of Arkansas Student Undergraduate Research Fellowship (SURF) grant, $3,900, January 2008 – October 2008.
4) **S. C. Smith (50%)**, J. Di (25%), and W. K. Al-Assadi (25%), "Collaborative Research: Integrating Asynchronous Digital Design into the Undergraduate Computer Engineering Curriculum throughout the Nation," NSF CCLI Phase II, DUE-0717572 and DUE-0717767, $499,999, August 2007 – July 2011.
5) G. K. Venayagamoorthy (65%), **S. C. Smith (20%)**, and K. A. Corzine (15%), "GAANN: Advanced Computational Techniques and Real-Time Simulation Studies for the Next Generation Energy Systems," Department of Education, P200A070504, $360,000, June 2007 – May 2010.
6) **S. C. Smith (67%)** and W. K. Al-Assadi (33%), "Integrating Asynchronous Digital Design and Testing into the Undergraduate Computer Engineering Curriculum," NSF CCLI Phase I, DUE-0536343, $94,789, February 2006 – July 2007.
7) K. Krishnamurthy (50%) and **S. C. Smith (50%)**, "REU: Summer Research Experiences for Undergraduates in Micro Mechatronic Systems," NSF, EEC-0139117, $94,214, March 2006 – August 2007.
8) **S. C. Smith**, "Group Selection in a Senior/Graduate Level Digital Circuit Design Course," University of Missouri New Faculty Teaching Scholars, $686, April 2005 – September 2005.
9) **S. C. Smith**, "DSP Filtering for Wayside MUX," Quackenbush Engineering Solutions & Technologies (QuEST), LLC, $6,800, July 2004 – October 2004.
10) **S. C. Smith**, "Evaluation of a Dissolution Rate Monitor on Base-soluble Polymers," Brewer Science, Inc., $3,731, September 2003 – December 2003.
11) **S. C. Smith**, "Development and Speedup of Self-Timed Digital Circuits," University of Missouri Research Board, $23,400, January 2002 – May 2003.

HONORS & AWARDS:

1) Elected IEEE Senior Member (2006)
2) Appeared in Marquis Who's Who in Science and Engineering, 8th Edition (2005/2006)
3) Received Recognition of Teaching Excellence from the UMR Committee for Effective Teaching and Faculty Awards (2002/2003 Academic Year)

PROFESSIONAL DEVELOPMENT:

1) Participated in University of Arkansas's Baum Teaching Workshop (8/21/08)
2) Participated in University of Arkansas's New Faculty Luncheon & Discussion Program (2007 – 2009)
3) Attended seminar on "Conducting Research on Teaching and Learning in Engineering and the Sciences" (3/11/05)
4) Successfully completed the University of Missouri – Rolla Grant Writing Workshop (2004)
5) Successfully completed the University of Missouri New Faculty Teaching Scholars Program (2003)
   - Included three workshops on course design, effective teaching, and academic portfolio development
6) Successfully completed the NSF-sponsored Engineering Education Scholars Workshop (July 27-30, 2002)
   - Covered effective teaching techniques and grant writing
   - Participants were first year faculty and final year Ph.D. students
   - I was 1 of 32 selected to participate out of over 70 applicants
7) Participated in UMR's New Faculty Forum Program (2001 – 2002)